

# MODELLING THE NOISE PROPERTIES OF PSEUDOMORPHIC HEMTS

R.I. Taylor and A.J. Holden\*

## Introduction

Recently, there has been strong demand for low noise amplifiers operating in the cm-mm wave band. At 12 GHz, this demand has been driven by DBS applications, whereas at higher frequencies (>40 GHz) the demand has been driven by satellite communications for military applications. For both applications, the minimum noise figure of the device (which is effectively the ratio of output noise to input noise) is often the critical device parameter.

Short gate length (< 0.3  $\mu\text{m}$ ) InGaAs/GaAs pseudomorphic HEMTs (PSHEMTs) now have the capability of achieving the ultra-low noise figures demanded by systems engineers. To design such PSHEMTs, however, it is necessary to have a thorough understanding of how the noise properties of the PSHEMT depend on gate length, bias, frequency, and parasitic source and gate resistances.

## Details of Noise Modelling

The basic principles of noise modelling are common to FETs, HEMTs, and PSHEMTs for frequencies greater than 1 GHz. Three main steps are required :

1. Modelling the DC characteristics of the transistor, and evaluating the associated small signal parameters, such as transconductance and drain resistance.
2. Deriving expressions for the mean square drain and noise currents, and any correlation between the two.
3. Using the noise currents and DC characteristics to derive the equivalent circuit representation of the transistor. Simple circuit theory can then be used to obtain an expression for the minimum noise figure.

In general, such a calculation is carried out numerically. At low frequencies compared to the cut-off frequency, however, noisy transistors can be modelled reasonably accurately using the Fukui equation [1] :

$$F_{\min} = 1 + 2 \left( \frac{f}{f_t} \right) \sqrt{P g_m (R_s + R_g)} \quad (1)$$

---

\* R.I. Taylor and A.J. Holden are with Plessey Research Caswell, Caswell, Towcester, Northants, NN12 8EQ.

Here,  $f$  is the operating frequency,  $f_t = \frac{1}{2\pi} \left( \frac{g_m}{C_{sg}} \right)$ ,  $g_m$  is the transconductance,  $C_{sg}$  is the source-gate capacitance,  $R_s$  is the source resistance and  $R_g$  is the gate resistance.  $P$  is essentially a fitting factor in Fukui's theory. Equation (1) may be derived from the full noise modelling calculation if it is assumed that the intrinsic noise of the transistor channel is negligible, and that only terms linear in frequency need be retained. For  $\left( \frac{f}{f_t} \right) > 0.3$  the linear approximation begins to break down. In addition, for transistors with very low noise figures (e.g.  $< 1$  dB at 12 GHz), the largest contribution to the noise figure is due to intrinsic channel noise, and the Johnson noise contribution from the parasitic resistances is relatively minor. In both these technologically important cases, the assumptions underlying the Fukui equation break down, and the full noise model must be employed.

It is convenient to define the following dimensionless noise coefficients

$$P = \frac{\langle i_d^2 \rangle}{4kTg_m\Delta f} \quad ; \quad R = \frac{\langle i_g^2 \rangle}{4kT\omega^2 C_{sg}^2 \Delta f / g_m} \quad ; \quad jC = \frac{\langle i_g^* i_d \rangle}{\sqrt{\langle i_g^2 \rangle \langle i_d^2 \rangle}} \quad (2)$$

where  $i_g$ ,  $i_d$  are the gate and drain induced noise currents respectively, and  $\Delta f$  is the bandwidth. At high frequencies ( $> 1$  GHz),  $1/f$  noise sources are unimportant, and the transistor channel noise is mainly due to thermal noise of the carriers if the device is biased into the Ohmic part of the DC characteristic. If the device is biased into the saturated region, shot-like noise also contributes. In either case, the induced noise currents, and their correlation, may be calculated using Pucel's method [2].

## Results

The ultimate limit to the device noise performance occurs when the parasitic resistances vanish. As mentioned above, Fukui's equation breaks down since it predicts a 0 dB noise figure, whereas in practice the intrinsic channel noise of the transistor gives rise to a significant noise figure. Pucel's model [2] gives the following formula for the intrinsic channel noise :

$$F_{\min} = 1 + 2 \left( \frac{f}{f_t} \right) \sqrt{PR(1-C^2)} \quad (3)$$

Under low noise bias conditions, Cappy [3] reports that  $P \approx 1.0$ ,  $R \approx 0.5$ , and  $C \approx 0.85$ . The main difference in the noise performance of FETs, HEMTs, and PSHEMTs then arises from the different "figure of merit" of these devices (the figure of merit is  $f_t L$ , where  $L$  is the gate length). Hikosaka [4] reports that  $f_t L = 18$  GHz  $\mu\text{m}$ , 21 GHz  $\mu\text{m}$  and 26 GHz  $\mu\text{m}$  for conventional AlGaAs/GaAs HEMTs, InGaAs/GaAs PSHEMTs, and InGaAs/InAlAs HEMTs

respectively. Assuming  $f_t L = 21$  GHz  $\mu\text{m}$ , Figures One and Two show the noise figure versus gate length for a PHEMT, for  $(R_s + R_g) = 0,3,6 \Omega$ , at frequencies of 12 and 40 GHz. At 12 GHz, the intrinsic noise of a  $0.3 \mu\text{m}$  PHEMT is 0.5 dB, which is a large fraction of the experimental value of 0.8-0.9 dB. This intrinsic channel noise can be decreased by shortening the gate and/or using an alternative materials system with a larger figure of merit.

In addition, the noise figure of a  $0.3$  and  $0.6 \mu\text{m}$  PHEMT has been calculated (under low noise conditions) as a function of frequency for  $(R_s + R_g) = 0,3,6 \Omega$ . The results are shown in Figures Three and Four. Clearly, at high frequencies, a linear dependence of  $F_{\text{min}}$  on frequency, as predicted by Fukui's equation [1] is inadequate.

Away from the low noise bias point, the values of the dimensionless noise coefficients differ from the values assumed above. The full noise model must be used to determine the variation of  $F_{\text{min}}$  versus current for fixed gate voltage, and Figure Five shows such a variation for  $0.5 \mu\text{m}$  PHEMT for various values of the parasitic resistances. This illustrates the important point that decreasing the parasitics also decreases the sensitivity of  $F_{\text{min}}$  to current variations about the low bias point.

### Conclusions

The limitations of Fukui's equation in predicting  $F_{\text{min}}$  for very low noise PHEMTs, and/or at high frequencies has been discussed. The limits to PHEMT noise performance are due to the intrinsic channel noise of the carriers, and the variation of this ultimate noise limit has been calculated for various gate lengths and frequencies. Finally, it has been shown that decreasing the parasitic resistances causes a decrease in sensitivity of the PHEMT noise figure to variations about the low noise bias point.

### Acknowledgements

This work has been supported and sponsored by the EC through the ESPRIT Basic Research Action program (BRA 3017).

### References

- [1] H. Fukui, "Optimal noise figure of microwave GaAs MESFETs", IEEE Trans. Elect. Dev., ED-26, 1032-1037, (1979)
- [2] R.A. Pucel, H.A. Haus, H. Stutz, "Signal and noise properties of GaAs microwave field effect transistors", Adv. Elect. & Elect. Phys., 38, New York : Academic Press, 195-265, (1975)
- [3] A. Cappy, "Noise modelling and measurement techniques", IEEE Trans. Micro. Theory. Tech., 36, 1-10, (1988)
- [4] K. Hikosaka, S. Sasa, N. Harada, S. Kuroda, "Current-gain cutoff frequency comparison of InGaAs HEMTs", IEEE Elect. Dev. Lett., 9, 241-243, (1988)

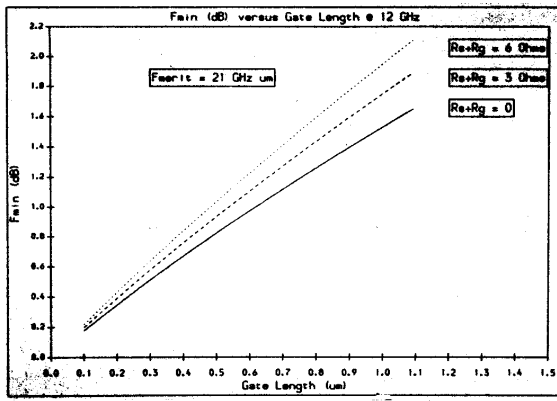


Figure One : Noise Figure (dB) versus gate length ( $\mu\text{m}$ ) for a PSHEMT at 12 GHz

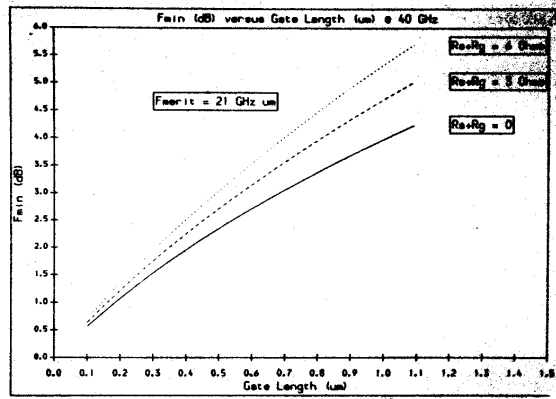


Figure Two : Noise Figure (dB) versus gate length ( $\mu\text{m}$ ) for a PSHEMT at 40 GHz

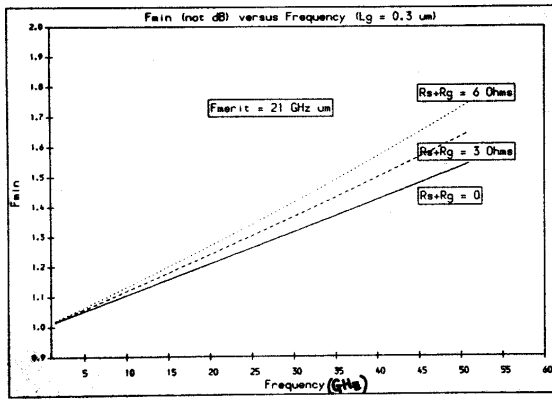


Figure Three : Noise figure (not in dB) versus frequency (GHz) for a  $0.3 \mu\text{m}$  PSHEMT

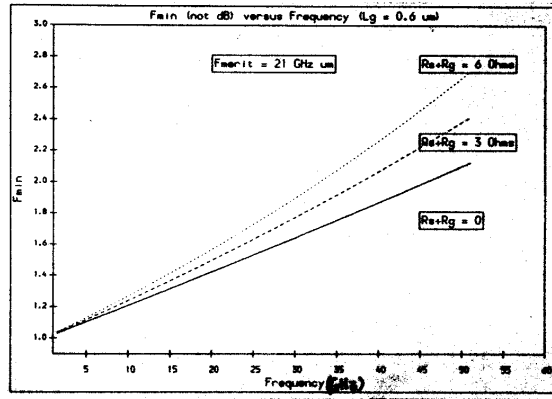


Figure Four : Noise figure (not in dB) versus frequency (GHz) for a  $0.6 \mu\text{m}$  PSHEMT

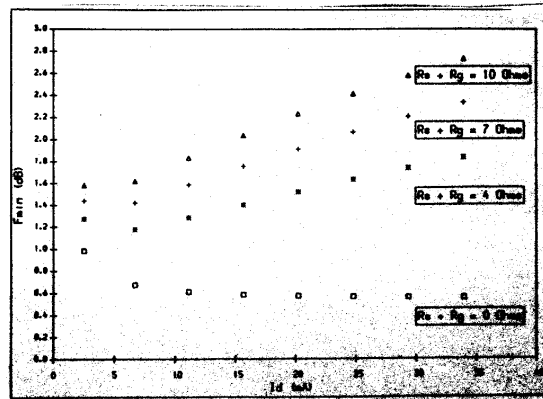


Figure Five : Noise Figure (dB) versus drain current (mA) for a  $0.5 \times 200 \mu\text{m}^2$  PSHEMT at 12 GHz